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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,210	12/10/2003	Robert John Allen	YOR920030406US1 (8728-649)	8018
46069	7590	03/23/2005	EXAMINER	
F. CHAU & ASSOCIATES, LLC 130 WOODBURY ROAD WOODBURY, NY 11797			DINH, PAUL	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/733,210

Applicant(s)

ALLEN ET AL.

Examiner

Paul Dinh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 February 2005.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
4a) Of the above claim(s) 13-15 is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-12 and 16-27 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 10 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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DETAILED ACTION

This is a response to the applicant election filed on 2/9/05. The examiner acknowledges:

The Applicants election of group I (claims 1-12 and 16-27) with traverse; thus claims 13-15 are non-elected.

Claims 1-27 are pending.

Election/Restriction Requirement Issue.

Applicant's election of group I for prosecution with traverse is acknowledged. The grounds for traverse are, as stated by the applicant: (A), the invention must be independent or distinct as claimed; and (B) there must be a serious burden on the examiner.

The traverse has been fully considered, and is not found persuasive because:

Due to different subject areas in the claimed groups, proper search and proper examination of the entire application cannot be made without serious burden on the examiner.

The issue of serious burden on the examiner is one part of restriction requirements; the other issue of restriction requirements that made the restriction required is because the application has 2 claimed groups that distinctly involve 2 different subject areas. Specifically group I drawn to a method for hierarchical design, group II drawn to a method for processing a design graph. Different subject matter of these 2 groups required searches in different areas.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

The restriction requirement has been fully considered, fully reconsidered, **the requirement is still deemed proper and is therefore made FINAL**. The elected claims 1-12 and 16-27 will be examined in this office action; the non-elected claims 13-15 are withdrawn from consideration pursuant to 37 CFR 1.142(b), as being nonelected. The applicants are advised that cancellation of non-elected claims is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-8, 12, 16-23, 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Lipton et al (USP 6505323)

(Claims 1, 16)

representing a structure of a hierarchical VLSI design as a graph (col 2-5, 13-14, fig 8-27) comprising design objects;

specifying a transformation behavior (col 1 lines 31-33, col 2-3, col 32, fig 8-27) applied to the design objects; and

processing, top-down, the graph to perform the transformation on the hierarchical VLSI design (col 2-5, 13-14, fig 8-27).

(Claims 2, 17) wherein the processing further comprises searching for an isomorphic structure (Col 2 lines 21-28, col 3 line 40, col 4 line 41-42).

(Claims 3, 12, 18, 27) wherein the graph describes a plurality of scopes, wherein each scope comprise an internal node and a leaf node (col 5-6, fig 13-21)

(Claims 4, 19) wherein the graph is based on a point set interaction between structures of the hierarchical very large scale integration design (fig 1-34).

(Claims 5, 20) wherein the graph is based on symmetry groups between structures of the hierarchical VLSI design wherein the graph represents a circuit substructure (col 2-4, summary, fig 9-21).

(Claims 6, 21) wherein an attribute is attached to a design object, the attribute having a user-defined mapping between an attribute transformation and a design object transformation (col 30 line 29+, col 31 line 15+).

(Claims 7, 22) wherein processing, top-down, comprising transcending information from a child graph to a parent graph, wherein a node in the parent graph represent an instance of the child graph (fig 3-4, 8, 13-16, 22-27, 31, col 5-6, 8).

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(Claims 8, 23) wherein processing, top-down, the graph comprises resolving boundary conditions, recursively, by adjusting a parent cell, beginning with a root cell of the graph (fig 3-4, 12-19, 23-32).

2. Claims 1, 8-11, 16, 23-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Aubel et al (USP 5696693)

(Claims 1, 16)

representing a structure of a hierarchical VLSI design as a graph (fig 4-8) comprising design objects;

specifying a transformation behavior (col 2 line 42+) applied to the design objects; and

processing, top-down, the graph to perform the transformation on the hierarchical VLSI design (col 2 line 42+).

(Claims 8, 23) wherein processing, top-down, the graph comprises resolving boundary conditions, recursively, by adjusting a parent cell, beginning with a root cell of the graph (fig 4-8).

(Claims 9-10, 24-25) wherein each cell is represented by a plurality of connected least enclosing orthogonal point sets (col 2 line 2+); determining an interaction between the least enclosing orthogonal point sets (col 2 line 2+); and determining a decomposition of the cell according to the interaction.

(Claims 11, 26) wherein processing, top-down, further comprises cloning by expression using a result of the decomposition to produce a cell definition (col 6 lines 66-67)

3. Claims 1 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Kale et al (US patent Application Publication No. 2004/0010759)

representing a structure of a hierarchical VLSI design as a graph (para 0088, 0129) comprising design objects;

specifying a transformation behavior (para 0047, 0066, 0085) applied to the design objects; and

processing, top-down, the graph to perform the transformation on the hierarchical VLSI design (para 0088, 0129).

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh

Patent Examiner

Paul Dinh
3/17/05